Toward 300 mm Wafer-Scalable High-Performance Polycrystalline Chemical Vapor Deposited Graphene Transistors

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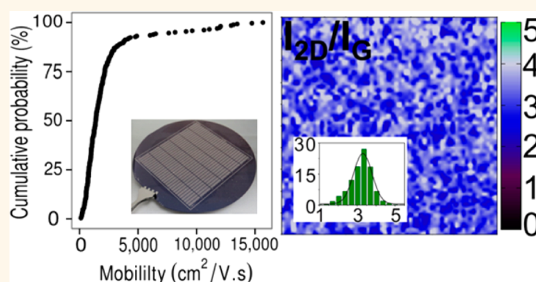
ABSTRACT The largest applications of high-performance graphene will likely be realized when combined with ubiquitous Si very large scale integrated (VLSI) technology, affording a new portfolio of "back end of the line" devices including graphene radio frequency transistors, heat and transparent conductors, interconnects, mechanical actuators, sensors, and optical devices. To this end, we investigate the scalable growth of polycrystalline graphene through chemical vapor deposition (CVD) and its integration with Si VLSI technology. The large-area Raman mapping on CVD polycrystalline graphene on 150 and 300 mm wafers reveals >95% monolayer uniformity with negligible defects. About 26 000 graphene field-effect transistors were realized, and statistical evaluation indicates a device yield of ∼74% is achieved, 20% higher than previous reports. About 18% of devices show mobility of >3000 cm^2/(V s), more than 3 times higher than prior results obtained over the same range from CVD polycrystalline graphene. The peak mobility observed here is ∼40% higher than the peak mobility values reported for single-crystalline graphene, a major advancement for polycrystalline graphene that can be readily manufactured. Intrinsic graphene features such as soft current saturation and three-region output characteristics at high field have also been observed on wafer-scale CVD graphene on which frequency doubler and amplifiers are demonstrated as well. Our growth and transport results on scalable CVD graphene have enabled 300 mm synthesis instrumentation that is now commercially available.



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Graphene, a two-dimensional sheet of carbon atoms, has attracted research attention on a wide variety of high-performance device applications owing to its remarkable electronic, optical, and mechanical properties.[1−13] The largest application of graphene will likely be realized when combined with ubiquitous Si complementary metal−oxide−semiconductor (Si CMOS) technology. However, the integration of graphene with Si CMOS has been a great challenge due to the lack of a reliable large-scale preparation scheme for graphene that preserves the high performance of the chip-scale graphene films. Several different methods have been proposed for growing wafer-scale graphene, including epitaxial growth on SiC wafers,[8,14] reduction of graphene oxide,[15,16] chemical vapor deposition (CVD) on metal thin films,[9,17] and recently CVD on hydrogen-terminated single-crystalline germanium surfaces.[10] Among these methods, the CVD mechanism is the most well-studied and reproducible mechanism and is more likely to be compatible with Si very large scale integrated (VLSI) technology. The CVD mechanism can be achieved on metal foils or films based on Cu, where the former (Cu foils) has been the most widely adopted method. However, the CVD growth of graphene on inexpensive and widely available Cu foils, while having great potential for roll-to-roll or flexible technology,[7,18,19] is not compatible with the Si CMOS integration process due to the lack of mechanical rigidity of Cu foils. On the other hand, deposited Cu films on standard oxidized silicon wafers that afford integration compatibility with Si VLSI previously suffered from uncontrolled polycrystalline structure that leads to defective graphene formation with inferior

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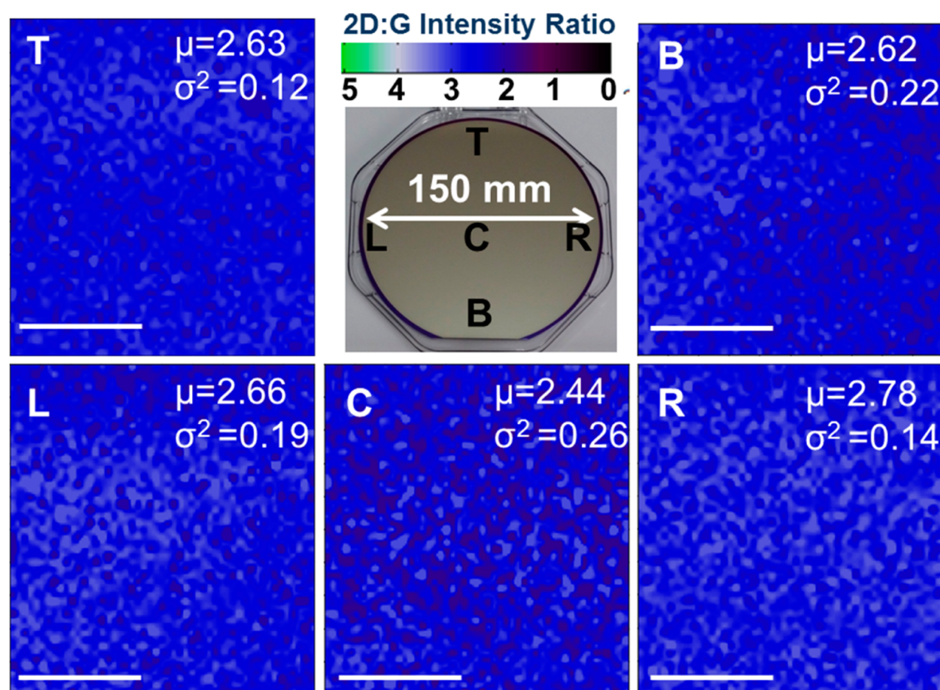

Figure 1. Large-area Raman mapping of graphene on 150 mm Cu substrates reveals >95% monolayer continuity and an average value of ∼2.62 for I_{2D}/I_G. The average value and the standard deviation of I_{2D}/I_G for each Raman map are presented. The view of the 150 mm wafer, used for this study, is shown at the top center of the image. The scale bar represents 200 μm.

performance, such as lower carrier mobility.[20] Recent progress revealed the growth of monolayer graphene with minimal defects by controlling parameters such as hydrogen or oxygen on the Cu surface to promote Cu(111) crystallization or to suppress graphene nucleation, resulting in the growth of large graphene domains across several Cu grains, respectively.[21,22] These studies suggest that the high quality of graphene synthesized on polycrystalline films is sufficient for device applications. Most remarkably, transport studies on polycrystalline graphene reported here offer higher peak mobility than recent reports on single-crystalline synthesized graphene.[8,10] This counterintuitive observation can be understood from theoretical and experimental analysis that suggests grain boundary scattering is likely not the dominant mechanism limiting charge transport in wafer-scale graphene devices.[23−25]

In this article, we demonstrate the scalability of CVD graphene growth on polycrystalline Cu films from 100 to 300 mm substrates and its integration with Si substrates for future VLSI integrated technology. The synthesized polycrystalline graphene offers a superior carrier transport characteristic to existing poly- or single-crystalline wafer-scale reports. Monolayer graphene coverage of >95% is achieved on 300 mm wafer substrates with negligible defects, confirmed by Raman mapping. Approximately 26 000 back-gated graphene field-effect transistors (GFETs) are realized by a CMOS-compatible fabrication method, and statistical evaluation of the electrical characteristics reveals a device yield of ∼74% was achieved, comparable to the 70−80% yield of early (1960s) silicon wafer-scale device development.[26] An average carrier mobility of ∼2113 $cm^2/(V\ s)$ was achieved, and notably ∼18% of devices showed mobility of >3000 $cm^2/(V\ s)$. The peak mobility observed here is ∼40% higher than the equivalent value reported for wafer-scale single-crystalline graphene so far. Low-temperature transport measurements show phonon scattering affects higher-mobility GFETs and impurity scattering is dominant for lower-mobility devices, suggesting that lowering the residual impurity level is critical for achieving high-performance devices. We also demonstrate frequency doubler and signal amplifier functions from wafer-scale devices as practical examples for large-scale analog electronics.

RESULTS AND DISCUSSION

The CVD graphene growth, demonstrated on 100 mm wafers[12] at 975 °C, has been scaled to 150 mm (Figure 1) and 300 mm (Figure 2) wafers using a CH_4 precursor at 750−800 °C (see Methods and Figure S1 for growth details). The reduction in the growth temperature has been achieved by employing both a substrate and a showerhead heater, leading to a more uniform heating of the gas flux in the vertical and lateral directions. The homogeneous heat distribution in the growth chamber is critical in order to produce graphene with low defect density and uniform quality all across the 300 mm wafer (see the Supporting Information). A hydrogen-saturated annealing step is

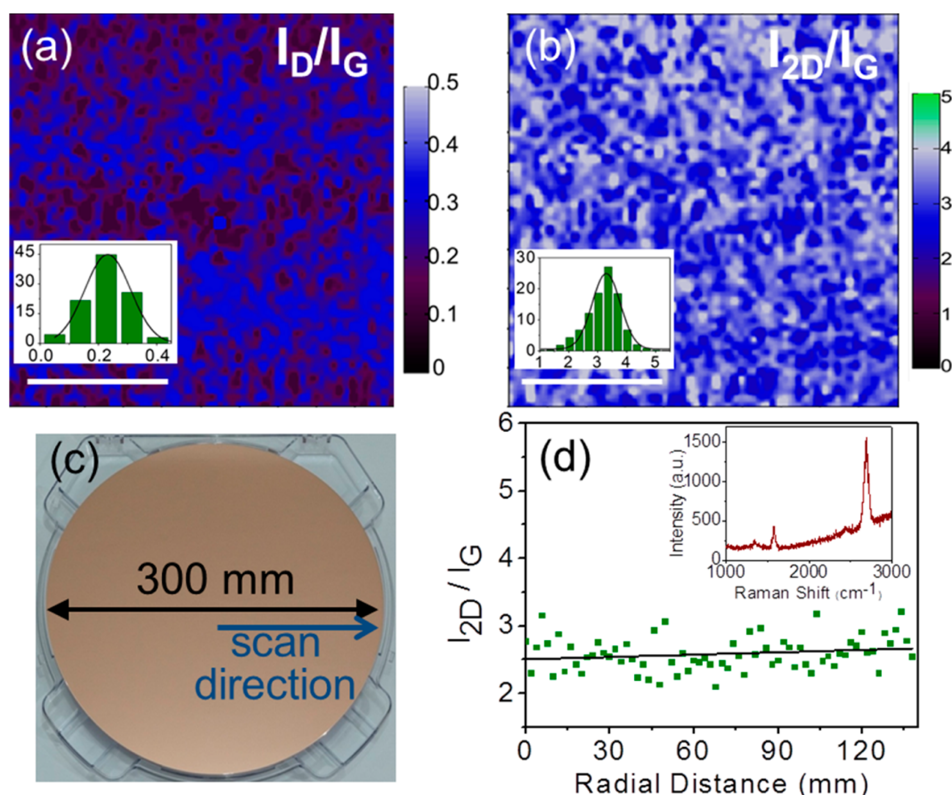

Figure 2. (a) I_D/I_G and (b) I_{2D}/I_G Raman mapping at the center of a 300 mm growth substrate shows the high quality of graphene with a negligible defect peak. The insets are the histogram distributions of I_D/I_G and I_{2D}/I_G, with average values of 0.2 and 3.4, respectively. Scale bars are 50 μm. (c) View of the 300 mm substrate used for this study. Arrow shows the direction of the Raman spot scans. (d) I_{2D}/I_G of Raman spot scans performed along the radial direction of the 300 mm substrate. The inset shows a representative Raman spectrum.

performed on the uniformly heated substrate, to promote the growth of hexagonal-phase Cu(111) structures (~> 10 μm), and is followed by the growth step with CH_4 and without H_2, which subsequently leads to the formation of scalable monolayer graphene with negligible defect density.[21] A set of images of 100–300 mm Si substrates used for this study is shown in Figure S2.

To verify the uniformity of the grown film on 150 and 300 mm substrates, Raman spectroscopy mapping was employed (see Methods). Figure 1 shows the mapping results collected from five different locations of the 150 mm substrate (500 μm × 500 μm mapping area). The 2D:G intensity ratio (I_{2D}/I_G) on the mapped area shows an average value of ~2.62 with a standard deviation of 0.19. Mapping of the D:G intensity ratio (I_D/I_G) on the same locations, presented in Figure S3, shows an average value of 0.06 with a deviation of 0.008, indcating the good structural quality of the synthesized graphene. On the basis of the statistical analysis of the Raman mapping data, monolayer graphene was achieved on 150 mm substrates with negligible defects.

Similarly, Raman mapping confirmed uniform monolayer graphene with a negligible defect peak and average values of 0.2 and 3.4 for I_D/I_G and I_{2D}/I_G on an area of 150 μm × 150 μm at the center of a 300 mm substrate (Figure 2a and b). The view of the 300 mm substrate used for this study and the results of the Raman spot scans as a function of distance from the center of the wafer are shown in Figure 2c and d. An average value of 2.6 is achieved for I_{2D}/I_G spot scans along the radial direction, comparable to the average I_{2D}/I_G on a 150 mm substrate, confirming the scalability of the growth process.

Table 1 summarizes the results of Raman spectroscopy scanning obtained here and compares it to other extracted and reported values of I_{2D}/I_G and I_D/I_G from wafer-scale CVD and epitaxially grown poly- and single-crystalline graphene. The comparison shows the saturated hydrogen annealing and methane-only precursor for the growth step in this study leads to a larger value of I_{2D}/I_G, while I_D/I_G does not exhibit a significant increase with scale-up in the growth wafer substrate.

The wafer-scale graphene preserves its high quality after transfer from a 100 mm growth substrate to the same wafer size constrained by our 100 mm microelectronic device fabrication cleanroom. The Raman spot scans, taken from five different locations on the 100 mm SiO_2/Si substrate after the transfer, show a negligible defect peak and good quality across the 100 mm wafer (Figure 3a). For instance, the average value of I_{2D}/I_G after the transfer, presented in Figure 3b, shows a narrow distribution within 2.5–3 with negligible

TABLE 1. Comparison of the Material and Electrical Properties of Reported Wafer-Scale Polycrystalline and Single-Crystalline Graphene

substrate/size (mm)	I_{2D}/I_G	I_D/I_G	μ_{max} (cm^2/(V s))	residual carrier density ($\times 10^{11}$ cm^{-2})	ref
Cu film/100−300	2.6−3.3	0.03−0.22	15 660	3.4−29	this work
Cu film/200	1.8	0.13	3800	1.49[d]	Gao, 2014[11]
Ge(110)[a]/50	3.5	0.03	10 600	3[d]	Lee, 2014[10]
SiC[a]/ 100	1.6−1.9	0[b]	2700	10−100	Kim, 2013[8]
Cu film/100	3	0.2	4900	10[d]	Tao, 2012[12]
Cu film/150	4.5	0.3	23 000[c]	10−40	Heo, 2011[13]
Ni/Cu films/75	3.5	0.25	3000	28[d]	Lee, 2010[9]

[a] Single-crystalline substrates. [b] Graphene structures always contain a finite defect peak.[37] No defect peak was reported; as such, this reported value is likely to be incorrect. [c] Only 3% of measured devices showed $\mu > 3000$ cm^2/(V s). [d] Data are based on single device report.

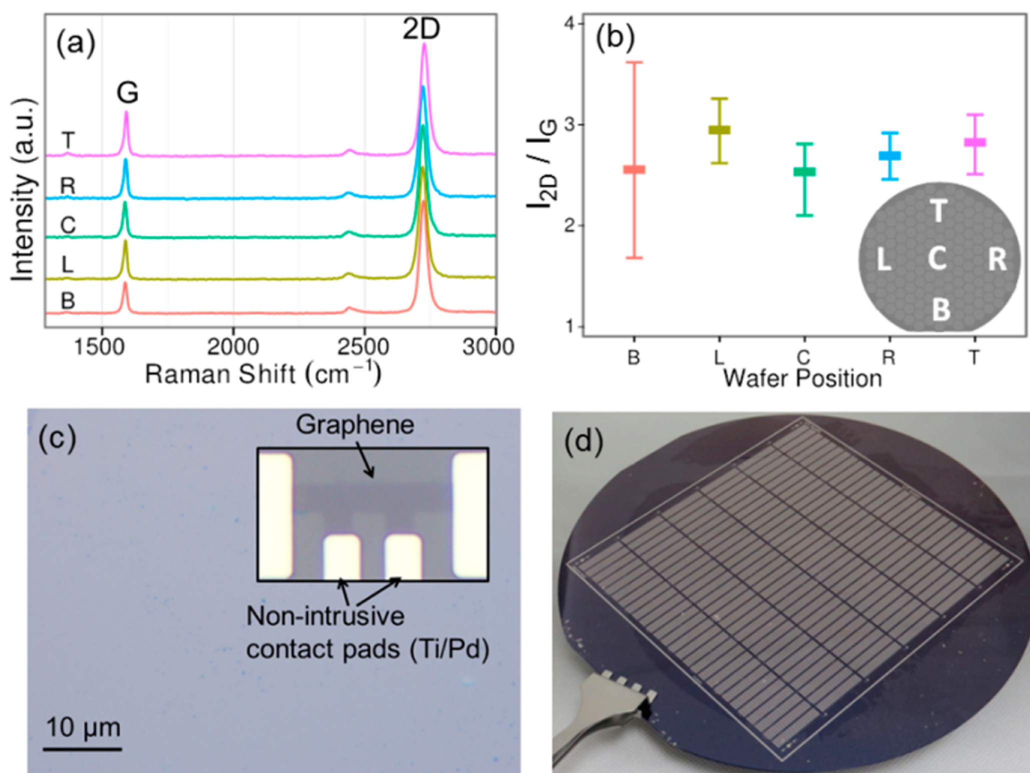

Figure 3. (a) Raman spot scans of graphene after transfer to a 100 mm wafer showing negligible defect mode. The Raman spectra were normalized to the intensity of the 2D peak before stacking. (b) The statistical distribution of I_{2D}/I_G at five different locations on the 100 mm substrate shows good uniformity. (c) Optical image of graphene after the transfer. The inset shows a representative four-probe device. (d) View of 26 000 fabricated graphene devices on a 100 mm Si wafer.

defect ratio. A microscopic image of the graphene film after the transfer to SiO_2/Si substrate and the view of the 100 mm substrate after device fabrication are presented in Figure 3c and d.

Using a standard UV photolithography method, about 26 000 back-gated GFETs were fabricated on the transferred film (see Methods for fabrication steps). A variety of two- and four-probe back-gated GFETs with varying length and width (3, 6, and 9 μm) were fabricated to investigate the electrical characteristics of the graphene channels. An optical image of a fabricated four-probe device (W = 3 μm, L = 9 μm) with nonintrusive contact pads is shown in the inset of Figure 3c.

Due to the long time required for performing the field-effect modulation by sweeping the back-gate bias in the [−30, 30] V range on every fabricated GFET, a statistical study was carried out on 550 randomly chosen GFETs across the wafer. A device yield of 74% with a confidence interval (margin of error) of 3.7% was achieved, a 20% higher yield than prior work.[13] The low value of the confidence interval indicates that if all devices had been tested, the device yield would be in the range of 74 ± 3.7% with 95% probability (see Supporting Information). The distributions of the field-effect mobility, Dirac voltage (V_{Dirac}), contact resistance ($R_{contact}$), and sheet resistance (R_{sheet}) under ambient conditions, in the form of cumulative

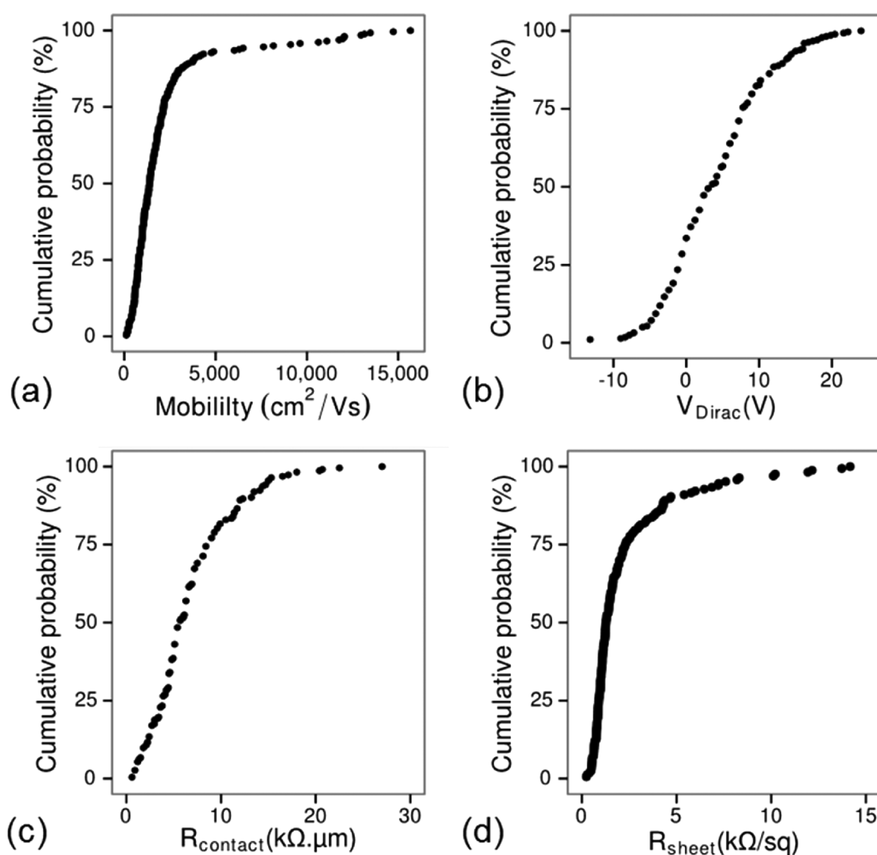

Figure 4. Cumulative plots of (a) field-effect mobility (mean: 2113 $cm^2/(V\ s)$), (b) V_{Dirac} (mean: 6.2 V), (c) $R_{Contact}$ (mean: 2116 $\Omega\cdot\mu m$), and (d) R_{sheet} (mean: 2600 Ω/sq). The device arrays have dimensions in the micrometer range, and all measurements are performed under ambient conditions.

probability plots, are presented in Figure 4a–d. The average value of the field-effect mobility, which is extracted using a widely accepted diffusive transport model,[27] is observed to be 2113 $cm^2/(V\ s)$, and most notably the mobility of 5% of GFETs is above 10 000 $cm^2/(V\ s)$, 5 times higher than prior results over the same range.[13] These values of mobility are comparable to the mobility values extracted from high-quality chip-scale polycrystalline CVD graphene samples[25,28] and epitaxially grown graphene on a wafer-scale single-crystalline substrate.[8,10] The high percentage of devices with $\mu > 10\,000$ $cm^2/(V\ s)$ achieved here is further evidence of the previous reports that high carrier mobility mainly correlates with graphene domain structures generated during the synthesis process rather than graphene domain size.[23–25] The statistical 5–95% mobility and $R_{contact}$ distribution at five different locations of a 100 mm wafer are presented in Figure S4a,b. The comparison between Figure S4a and b suggests that regions with lower average $R_{contact}$ show higher average mobility values. Considering the Raman spot scans, after the transfer (Figure 3b), the variation of mobility and $R_{contact}$ distribution at different locations on the wafer after the fabrication process is believed to be mainly due to the resist residue rather than initial differences in the quality of graphene.[29] The high value of the average mobility, achieved here, is a promising indicator that the likely success of ongoing integration research in addressing the sources of electrical variability, coming from the residue of the transfer and fabrication process, will result in uniformly high-performance graphene devices at wafer scale. It is also worth noting here that the dimensions of the largest channels (3 μm × 9 μm) are smaller than the average domain size of the synthesized film (∼> 10 μm) obtained by our growth process. We expect that, with similar likelihood, the transistor channels traverse graphene domain boundaries or are contained within a single graphene domain.

The Dirac voltage, presented in Figure 4b, is narrowly distributed around 0 ± 10 V and shows an average value of 6.2 V. The positive and negative shifts of V_{Dirac} around 0 V are indicative of the slight p- and n-doped channels, which are believed to be caused by the net effect of moisture adsorption and photoresist impurities from the fabrication process[30–32] and the doping from the SiO_2 substrate.[33] The contact resistance, obtained by fitting the channel resistance *versus* the gate voltage, has an average value of 2116 $\Omega\cdot\mu$m, comparable to the reported Pd-based graphene–metal contacts fabricated by electron-beam

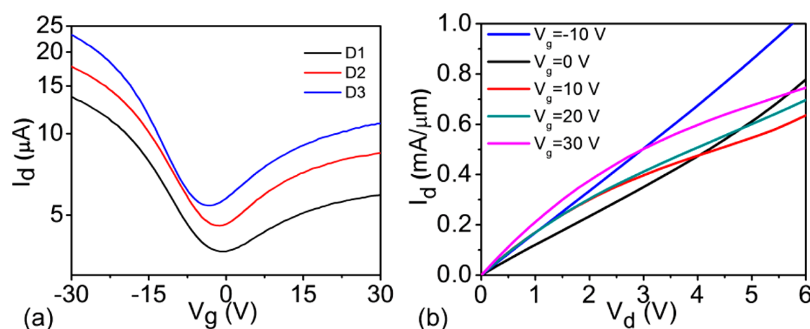

Figure 5. (a) Channel current *vs* gate voltage for three representative two-probe devices (D1: $W = 3\ \mu$m, $L = 3\ \mu$m; D2: $W = 6\ \mu$m, $L = 3\ \mu$m; and D3 $W = 9\ \mu$m, $L = 3\ \mu$m) at room ambient and V_d = 100 mV; mobilities are in the 2000−2500 cm^2/(V s) range. (b) I_d−V_d characteristics of a high-mobility device ($W = 6\ \mu$m, $L = 3\ \mu$m), μ = 10 600 cm^2/(V s), and V_{Dirac} = 0 V, at different back-gate voltage showing the intrinsic soft saturation of graphene.

(e-beam) lithography,[18,29,34] suggesting that the performance of the graphene−metal contact does not change drastically when the low-throughput e-beam lithography method is replaced by the CMOS-compatible UV photolithography at wafer scale. The sheet resistance, measured at floating back-gate potential, has an average value of 2600 Ω/sq, comparable to 1−2 kΩ/sq reported for the chip-scale CVD polycrystalline graphene devices.[35] The cumulative plot of sheet resistance measured at back-gate voltage 0 V and average V_{Dirac} of 6 V, shown in Figure S5, follows the same distribution of R_{sheet} at floating back-gate potential with larger average values, indicating smaller carrier density.

In Table 1 we compare the peak mobility (μ_{max}) at T = 300 K and the impurity density obtained here with other wafer-scale poly- and single-crystalline CVD and epitaxially grown graphene reported previously. The impurity densities listed in Table 1 for Kim *et al.*,[8] Lee *et al.*,[10] and Heo *et al.*[13] are exact reported values, and the listed values for Lee *et al.*,[9] Gao *et al.*,[11] and Tao *et al.*[12] are extracted through the equation $n \cong C_{ox}|V_g - V_{Dirac}|/e$, for nonzero V_{Dirac}, where V_g and e are the gate bias and the electron charge, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance per area, and ε_{ox} and t_{ox} are the gate dielectric and thickness, respectively.[36] The impurity density of measured devices here, which falls in the range of (3.4−29) × 10^{11} cm^{-2}, is extracted through a diffusive transport model and indicates the relatively low concentration of impurities in the synthesized graphene. The value of μ_{max} is one of the highest reported values for polycrystalline graphene so far and is ∼40% higher than the best value reported for single-crystalline graphene. Note that except for the data reported in this work and in Lee *et al.*,[9] Heo *et al.*,[13] and Lee *et al.*,[10] the rest of the reported values in Table 1 are based on a limited number of measurements performed on devices fabricated using e-beam lithography.

In the discussion to follow, we further evaluate the results of the electrostatic and transport properties of GFETs at low temperature and room ambient.

Figure 5a presents the drain current (I_d) of three representative GFETs, with varying width (3, 6, and 9 μm) and uniform length (3 μm), as a function of applied gate voltage at V_d = 100 mV and room ambient. The asymmetry between the hole and electron transport, observed mainly for two-probe GFETs in the 78−300 K range, possibly originates from pinning of the charge density below the metal contacts[38] and the higher scattering rates of electrons in the channel by the impurities.[30,31] Figure 5b presents I_d *versus* drain voltage (V_d) characteristics of a two-probe GFET (W = 6 μm, L = 3 μm) at different V_g. The soft saturation region, which reflects the ambipolar nature of graphene, was previously reported for exfoliated flakes mainly with top-gated structures.[39−41] We recently reported this effect on our high-mobility inductively heated synthesized CVD graphene on a 300 nm SiO_2 back-gate dielectric.[6] The current saturation effect is shown to be pronounced in high-mobility GFETs with low contact resistance.[42] The observation of this effect along with the kink effect in our wafer-scale GFETs indicates the high intrinsic quality of the grown graphene.

The temperature-dependent mobility of electrons and holes and the transport curves of a representative GFET (W = 3 μm, L = 9 μm) at 78−300 K are presented in Figure 6a and b and Figure S6. The observed mobility increases by ∼20% when the temperature is reduced to 78 K, suggesting that electron−phonon scattering is a significant scattering mechanism. A second device with lower room-temperature mobility and higher residual carrier density showed weaker dependence (∼5%) on temperature for the same range (Figure S7a,b). This suppressed temperature-dependence behavior suggests that the dominant scattering mechanism is likely to be charged impurities.[36,43] We observed a more symmetric V-shape transport characteristic from the four-probe GFETs after high vacuum (10^{-6} Torr) pumping for several hours (Figure S7c), resulting in the desorption of moisture and volatile adsorbates.[44]

Given the high average carrier mobility and demonstrated current saturation at room ambient, the

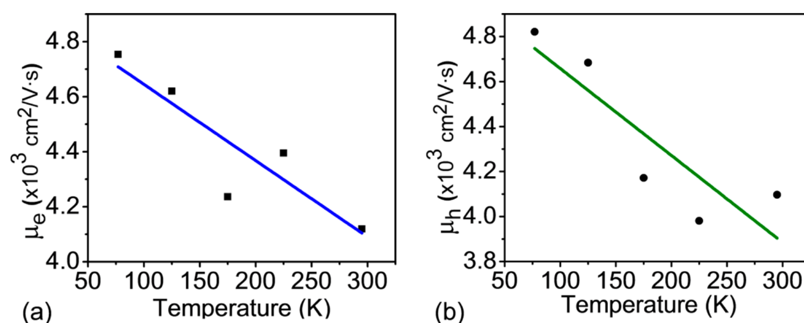

Figure 6. (a) Temperature dependence of (a) electron mobility (μ_e) and (b) hole mobility (μ_h) of a representative four-probe GFET (W = 3 μm, L = 6 μm) from 78 to 300 K. Transport curves of this device and a second GFET from 78 to 300 K are shown in Figures S5 and S6.

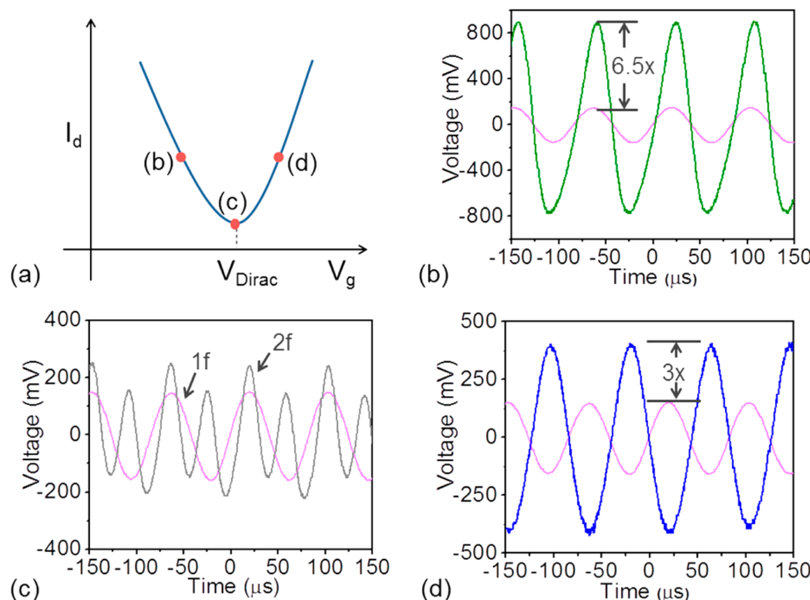

Figure 7. (a) Schematic of an I_d-V_g curve showing the corresponding applied gate bias for (b) noninverting amplification, (c) frequency doubler, and (d) inverting amplification. The pink curve represents the input signal.

wafer-scale high-performance GFETs are suitable for analog applications such as amplifiers and nonlinear high-frequency devices.[45−47] A triple-mode single-transistor amplifier is demonstrated based on the wafer-scale back-gated GFETs. Examples of a frequency doubler and noninverting and inverting common-source amplifiers are presented in Figure 7b−d. A schematic of the circuit is presented in Figure S8. The supply voltage, V_{DD}, was set to 500 mV for low-power operation with a load impedance of 1 MΩ. V_g is the combination of a fixed dc voltage and a small sinusoidal ac signal provided by a function generator. The input frequency, which is limited by the measurement setup, was 12 kHz. The gate bias of the GFET was adjusted to be in the hole or electron branch or ambipolar point for noninverting or inverting common-source amplifiers or frequency amplification, respectively (Figure 7a). Here a 6.5× voltage gain for the hole branch (Figure 7b), with the expected noninverting amplifier response, and a 3× gain for the electron branch (Figure 7d), between the output (at the drain) and input (at the gate), are demonstrated. The mismatch in the gain of the electron and hole branch is possibly due to the asymmetry of the transport characteristics of the device at room ambient. Once the device was biased at the minimum conduction point, the input signal sees a positive gain in its positive phase and a negative gain in its negative phase, resulting in frequency doubling. Figure 7c demonstrates the frequency doubling with an input signal of 12 kHz and output signal of 24 kHz.

CONCLUSIONS

In summary, we have demonstrated the state-of-the-art on scalable CVD polycrystalline graphene synthesis, device yield, and electrical statistics featuring outstanding wafer-scale devices with performance benchmarking exceeding that of previous wafer-scale polycrystalline graphene and recent reports on CVD single-crystalline graphene on hydrogen-terminated germanium substrates and epitaxially grown graphene on SiC substrates. The successful integration of CVD

graphene on a wafer scale is achieved by not only enhancing the performance of individual graphene devices but also uniform performance across many devices. Importantly, graphene with high material quality has been scaled from 100 mm to state-of-the-art 300 mm commercial Si wafers, which addresses one of the grand challenges for a future graphene–Si nanotechnology. Our CMOS-compatible device fabrication process achieved a yield of 74% with charge mobility, contact resistance, and sheet resistance superior to existing reports on the wafer-scale GFETs. The observation of a soft saturation effect and the demonstration of frequency doubler and analog amplifiers based on wafer-scale graphene make GFETs suitable for analog and high-frequency circuit applications.

METHODS

Synthesis and Transfer. The graphene synthesis procedure was carried out in an AIXTRON BM300T CVD system with a cold-wall chamber and a substrate and a showerhead heater setup at 750–800 °C for 300 mm graphene synthesis. The growth substrates consist of ~500–900 nm copper film on commercially available 300 nm thermally grown SiO_2 on a Si wafer. The complete graphene growth processing time on 300 mm wafers is 22 min including 2 min of annealing (H_2 ambient, flow rate 1000 sccm, pressure 25 mbar) and 3 min of growth (CH_4 ambient, flow rate 10 sccm) with an automated wafer transfer in and out of the process chamber at 600 °C.

Raman spectroscopy mapping data on graphene grown on 150 mm Cu substrates are collected using a 442 nm laser (Renishaw inVia) with a focal point size of 2 μm and on 300 mm substrates using a 457 nm laser with a focal point size of 0.9 μm, under ambient conditions. Mapping data were analyzed using GRISP software (https://nanohub.org/tools/grisp/).[48]

Graphene grown on a 100 mm substrate was transferred to a 90 nm SiO_2 substrate by selective etching of a Cu film using an ammonium persulfate ($(NH_4)_2S_2O_8$) aqueous solution. A 200 nm thick PMMA film (M_w 495 000 from Sigma-Aldrich) was used as a support layer for transferring the graphene to a SiO_2 substrate.

Device Fabrication and Analysis. The device fabrication was performed in our 100 mm cleanroom line. The graphene is coated with a 450 nm thick positive photoresist, Microposit S1805, and patterned using the UV photolithography process followed by O_2 plasma etching (200 mbar, 50 W) for 50 s. The metal stack of 2 nm Ti and 48 nm Pd is deposited by lift-off with 300 nm lift-off resist (Microchem LOR 3B) and 450 nm S1805 positive resist at room temperature.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Table S1. Temperature readings of sensors located at three different regions of the substrate. Figure S1. Process steps for growing graphene and their corresponding time scales. Figure S2. Images of the 100 to 300 mm substrates used for growing graphene. Figure S3. Large-area Raman mapping of graphene on 150 mm Cu substrates. Figure S4. 5–95% distributions of mobility and $R_{contact}$ at five locations on a 100 mm wafer. Figure S5. Sheet resistance of ~70 GFETs measured at different back-gate voltages. Figure S6. Electrical transport curves at different temperature steps in the 78–300 K range. Figure S7. Temperature-dependence of electron mobility and hole mobility of a second four-probe GFET and electrical transport curves of the same device at different temperature steps in the 78–300 K range. Figure S8. Circuit schematic of GFET frequency doubler. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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